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FOR

COMPOSITE DIELECTRIC LAYERS

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COMPOSITE DIELECTRIC LAYERS

BACKGROUND

Cross-Reference to Related Application

[0001] This application is a continuation of co-pending U.S. Patent Application No. 10/215,130, filed August 8, 2002.

Field

[0002] Integrated circuit processing and, more particularly, to the patterning of interconnections on an integrated circuit.

Background

[0003] Modern integrated circuits use conductive interconnections to connect the individual devices on a chip or to send or receive signals external to the chip. Popular types of interconnection include aluminum alloy interconnections and copper interconnections.

[0004] One process used to form interconnections, particularly copper interconnections, is a damascene process. In a damascene process, a trench is cut in a dielectric and filled with copper to form the interconnection. A via may be in the dielectric beneath the trench with a conductive material in the via to couple the interconnection to underlying integrated circuit devices or underlying interconnections. In one damascene process (a "dual damascene process"), the trench and via are each filled with copper material by, for example, a single deposition.

[0005] A photoresist is typically used over the dielectric to pattern a via or a trench or both in the dielectric for the interconnection. After patterning, the photoresist is removed. The photoresist is typically removed by an oxygen plasma (oxygen ashing). The oxygen used in the oxygen ashing can react with an underlying copper

interconnection and oxidize the interconnection. Accordingly, damascene processes typically employ a barrier layer of silicon nitride Si_3N_4 directly over the copper interconnection to protect the copper from oxidation during oxygen ashing in the formation of a subsequent level interconnection. In intelayer interconnection levels (e.g., beyond a first level over a device substrate), the barrier layer also protects against misguided or unlanded vias extending to an underlying dielectric layer or level.

[0006] In general, the Si_3N_4 barrier layer is very thin, for example, roughly 10 percent of the thickness of the pre-metal dielectric (PMD) layer or interlayer dielectric (ILD) layer. A thin barrier layer is preferred primarily because Si_3N_4 has a relatively high dielectric constant (k) on the order of 6-7. The dielectric constant of a dielectric material, such as an interlayer dielectric, generally describes the parasitic capacitance of the material. As the parasitic capacitance is reduced, the cross-talk (e.g., a characterization of the electric field between adjacent interconnections) is reduced, as is the resistance-capacitance (RC) time delay and power consumption. Thus, the effective dielectric constant (k_{eff}) of a PMD layer or ILD layer is defined by the thin barrier layer and another dielectric material having a lower dielectric constant so that the effect of the high dielectric material typically used for the barrier layer (e.g., Si_3N_4) is minimized. Representative dielectric materials for use in combination with a barrier layer to form PMD or ILD layers include silicon dioxide (SiO_2), fluorinated silicate glass (FSG), and carbon-doped oxide (CDO).

[0007] As technologies advance, the distance (e.g., pitch) between interconnections decreases as more devices and more interconnections (e.g., interconnect lines) are formed on a structure. Thus, the effective dielectric constant (k_{eff}) of a PMD or ILD layer is significant.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] **Figure 1** is a schematic side view of a portion of a circuit substrate or interconnect layer on a substrate including a contact point and a barrier layer formed over the contact point.

[0009] **Figure 2** shows the structure of **Figure 1** following the formation of a dielectric layer on the barrier layer.

[0010] **Figure 3** shows the structure of **Figure 2** following the formation of an interconnection to the contact point.

[0011] **Figure 4** is a schematic side view of a portion of a circuit substrate showing a contact point and a barrier layer overlying the contact point.

[0012] **Figure 5** shows the structure of **Figure 4** following the introduction of a sacrificial layer and the formation of an interconnection to the contact point.

[0013] **Figure 6** shows the structure of **Figure 5** following the removal of the sacrificial layer.

[0014] **Figure 7** shows the structure of **Figure 6** following the introduction of a barrier layer around the interconnection.

[0015] **Figure 8** shows the structure of **Figure 7** following the introduction of a dielectric layer on the substrate.

[0016] **Figure 9** shows the structure of **Figure 8** following the introduction of a barrier layer on the substrate.

DETAILED DESCRIPTION

[0017] **Figures 1-3** illustrate a dual damascene process for forming an interconnection over a contact point. A contact point is, for example, a device on a substrate (e.g., gate, junction, etc.). Alternatively, in a multi-level interconnection device configuration, the contact point also includes an underlying interconnection (e.g., an interconnection line). A typical integrated circuit of a microprocessor may have, for example, five or more interconnection layers or lines stacked on one another, each insulated from one another by dielectric material.

[0018] **Figure 1** illustrates a cross-sectional, schematic side view of a portion of a circuit substrate structure. Structure 100 includes substrate 110 of, for example, a semiconductor material such as silicon or a semiconductor layer on an insulator such as glass. Substrate 110 includes contact point 120 on a surface thereof. In one embodiment, contact point 120 is a portion of an underlying interconnect line (e.g., a metal trench). A representative interconnect line is shown in dashed lines. Overlying contact point 120 and substrate 110, in one embodiment, is barrier layer 130. Barrier layer 130 is selected, in one embodiment, to be a material having a dielectric constant (k) less than on the order of about five. In the context of a contact point that is a copper interconnection (e.g., interconnection line), barrier layer 130 is selected to have relatively good copper diffusion characteristics (i.e., to inhibit copper diffusion). Barrier layer 130 is also selected such that it is a material that has an etch characteristic such that it may be selectively etched or retained during an etch operation involving barrier layer 130 or a subsequently introduced dielectric material, such as a dielectric material that, together with barrier material 130, will serve as a pre-metal dielectric (PMD) or interlayer dielectric (ILD) layer dielectric material. One material for barrier layer 130 is cubic boron nitride (CBN). Cubic boron nitride has a dielectric constant on the order of 4-4.5. Cubic boron nitride may be introduced by chemical vapor deposition (CVD) and tends to serve as an inhibitor of copper diffusion when used as the barrier material in the context of copper. Further, cubic boron nitride is selectively

etchable in, for example, a fluorine plasma. Still further, cubic boron nitride is a relatively high compressive stress material allowing, in one example, its use in conjunction with high tensile stress materials to minimize the effect of the tensile stress.

[0019] In one embodiment, barrier layer 130 of cubic boron nitride is introduced, according to current technologies, to a thickness on the order of 40 nanometers (nm) to 100 nm. The thickness is selected, in one example, to be sufficient to protect an underlying contact point 120 (e.g., copper interconnection line), but not to unacceptably increase the capacitance between contact point 120 and, for example, an overlying or adjacent interconnection (e.g., thickness selected to minimize the contribution of barrier layer 130 to k_{eff}).

[0020] Overlying barrier layer 130 in the illustration shown in **Figure 2** is dielectric layer 140. Dielectric layer 140 is, for example, a tetraethyl orthosilicate (TEOS), a plasma enhanced CVD (PECVD), SiO_2, a fluorinated silicate glass (FSG), or a carbon-doped oxide (CDO) deposited to a thickness on the order of approximately 700 nanometers according to current technologies. As described in more detail with reference to **Figures 4-9** and the accompanying text, dielectric layer 140 may also be an aerogel. The thickness of dielectric layer 140 will depend, in part, on size characteristics and scaling considerations for the device. Collectively, barrier layer 130 and dielectric layer 140 define a composite dielectric layer (e.g., PMD or ILD layer) having a composite or an effective dielectric constant (k_{eff}). In one embodiment, the contribution of the material selected for barrier layer 130 is less than 20 percent, in another embodiment, less than 10 percent of the k_{eff}. Once dielectric layer 140 is deposited and formed, the material may be planarized, for example, with a polish (e.g., chemical-mechanical polish).

[0021] Referring to **Figure 3**, following the introduction of dielectric layer 140, an opening is made to contact point 120. In one embodiment, the opening includes via 160 and trench 170 formed, for example, by sequential photolithographic patterning and

etching operations. Representatively, what is shown is a dual damescene process where via 160 and trench 170 are formed as the opening and are filled with conductive material 150 such as a copper material and the conductive material in trench 170 serves as an interconnection line. Thus, although not shown in the cross sectional view of **Figure 3**, trench 170 may extend into the page as viewed to act as a trench for a conductive material interconnection line to reside therein. In addition to conductive material of, for example, a copper material in via 160 and trench 170, one or more layers may be deposited along the sidewalls of via 160 and trench 170 to, for example, inhibit diffusion of the conductive material and/or improve adhesion of the conductive material.

[0022] Via 160 opening is made through dielectric layer 140 and barrier material 130. To form an opening through dielectric layer 140, a suitable etchant is selected that does not substantially react or disrupt underlying barrier material 130. In the case of a dielectric layer 140 of FSG and barrier layer 130 of cubic boron nitride, a suitable etchant to etch FSG is, for example, a $SiCl_4$ etch chemistry. With such an etchant, an etch of dielectric layer 140 will proceed through the material and substantially stop when barrier material 130 is exposed. A subsequent etch chemistry, such as a fluorine-based etch chemistry (e.g., HF, CF_4) can then be used to form an opening through barrier material 130 and expose contact point 120.

[0023] After exposing contact point 120, conductive material 150 is deposited in trench 170 and via 160. A suitable conductive material is, for example, a copper material deposited by a damascene process. Once conductive material 150 is deposited in trench 170 and via 160, the substrate may be planarized. The process described above may then be repeated for a subsequent interconnection layer or layers.

[0024] **Figures 4-9** describe a second embodiment. Referring to **Figure 4**, structure 200 in this embodiment includes substrate 210 having a contact point 220 on a surface thereof. Contact point may be, for example, a device or an interconnection formed over a substrate to one or more devices formed on or near the substrate.

[0025] Overlying contact point 220 (as viewed) on a surface of substrate 210 in the structure of **Figure 4** is barrier layer 230. Barrier layer 230 may be deposited, representatively, as a blanket over a portion, including the entire portion of the surface of substrate 210. Barrier layer 230 is selected to be a material having a dielectric constant (k) less than 5. In another embodiment, barrier layer 230 is a material selected to have good copper diffusion characteristics and etch selectivity. Cubic boron nitride is one material that has such characteristics. Barrier layer 230 of cubic boron nitride, in one example, has a thickness on the order 40 nm to 100 nm.

[0026] **Figure 5** shows the structure of **Figure 4**, following the introduction of sacrificial layer 240 and the formation of trench 270, via 260 and conductive material 250 within the trench and via. Sacrificial layer 240 may be, for example, a dielectric material such as SiO_2 or other material that may be patterned to the exclusion of barrier material 230. Sacrificial layer 240 is deposited to a thickness sufficient (perhaps after planarization) to accommodate a properly sized interconnection line (in trench 270) and contact (in via 260). One suitable thickness for sacrificial layer 240 according to current techniques is on the order of about 700 nanometers. As shown in **Figure 5**, conductive material 250 of, for example, copper material is formed in trench 270 and via 260 and contacts contact point 220.

[0027] **Figure 6** shows the structure of **Figure 5** following the removal of sacrificial material 240. In the embodiment, where sacrificial material 240 is an oxide (e.g., SiO_2) and barrier material 230 is cubic boron nitride, sacrificial material 240 may be removed, by dipping structure 200 in hydrofluoric acid. Alternatively, an etchant introduced without a photolithographic mask overlying a portion of sacrificial material 240 to protect the material from an etch chemistry may be used. As shown in **Figure 6**, following the removal of sacrificial material 240, conductive material 250, such as a copper material, remains exposed on substrate 210 of structure 200. In an embodiment where conductive material 250 is copper, the exposure of conductive material 250 by

removal of sacrificial material 240 may be done in an inert or oxygen-free environment to prevent oxidation of the copper material.

[0028] **Figure 7** shows the structure of **Figure 6** following the introduction of barrier layer 280. In one embodiment, barrier layer 280 is selected of a material having a dielectric constant less than 5. One suitable material is cubic boron nitride. In this case, both barrier layer 230 and barrier layer 280 are cubic boron nitride. As shown in **Figure 7**, barrier layer 280 completely surrounds conductive material 250.

[0029] In one embodiment, there may be many conductive structures such as conductive material 250 formed to various contact points on substrate 210. A representative pitch between such structures (reference number 255 in **Figure 6**) may be on the order of about 70 nanometers according to current technologies for interconnection lines. Accordingly, the thickness of barrier layer 280 is selected, in one embodiment, to be sufficient to surround conductive material 250 but thin enough to leave an area between conductive material structures exposed so as, for example, not to create voids between the structures. Where a pitch between conductive structures is on the order of about 70 nanometers, a thickness of barrier layer 280 may representatively be on the order of 30 to 40 nanometers.

[0030] **Figure 8** shows the structure of **Figure 7** following the introduction of dielectric layer 290. In one embodiment, dielectric layer 290 is introduced as a blanket layer over a portion, including the entire portion of the structure. Dielectric layer 290, in one embodiment, is selected to have a low dielectric constant, preferably a dielectric constant less than two (2). In one embodiment, dielectric layer 290 is an aerogel (XLK). Aerogel is described as a porous glass and can have a dielectric constant on the order of 1.1. Although aerogel has a low dielectric constant, it is known to have inferior mechanical properties, being weak and brittle.

[0031] In one embodiment, dielectric layer 290 of aerogel may be introduced as a liquid, possibly through the use of a solvent. The material may then be dried

(supercritical drying) to evaporate the solvent and form a solid dielectric material layer. Planarization may also be necessary to expose barrier layer 280 over conductive material 250 or to expose conductive material 250. In one embodiment, dielectric layer 290 of, for example, aerogel, and barrier layer 280 act as the substrate surface for additional layers. Collectively, barrier layer 230, barrier layer 280, and dielectric layer 290 define a composite dielectric layer (e.g., PMD or ILD layer) having a composite or an effective dielectric constant (k_{eff}). In one embodiment, the contribution of the material selected for barrier layer 280 and the material selected for barrier layer 280 is less than 20 percent, in another embodiment less than 10 percent, of the k_{eff}.

[0032] **Figure 9** shows the structure of **Figure 8** following the introduction of barrier layer 295 as, for example, a blanket over a portion, including the entire portion, the substrate surface. In one embodiment, barrier layer 295 is similar to barrier layer 230 in that it has a dielectric constant less than about 5 and acts as a suitable diffusion barrier for a conductive structure for which it may be in contact. It also may have relatively good etch selectivity relative to a dielectric material that, together with barrier layer 295, forms an ILD. In one embodiment, barrier layer 295 is cubic boron nitride as is barrier layer 280 and barrier layer 230. In this manner, dielectric 290 of, for example, aerogel is encapsulated by cubic boron nitride.

[0033] In the preceding detailed description, specific embodiments are described. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.